Industry Trends

Heterogeneous Compute

Key challenge: Programming & integration of accelerators

Cloud to Edge

Key challenge: Need for retargetability

AI Proliferation

Key challenge: Efficient ML acceleration and integration in the whole application
Vitis Unified Software Platform
From Hardware to Software Programmable

- 2012: Vivado
- 2018: OS and Firmware SDK
- 2019: SDSoc, Embedded
- 2019: SDAccel, Data Center (FaaS, Alveo)
- 2019: AI inference Acceleration
- 2019: Vitis Unified Software Platform

© 2020 Xilinx
Vitis: Unified Software Platform

Domain-specific development environment

Vitis accelerated libraries
- OpenCV Library
- BLAS Library
- Finance Library

Vitis core development kit
- Compilers
  - ARM, HLS, AI Engines
- Analyzers
- Debuggers

Xilinx runtime library (XRT)

Vitis target platform

Coming soon...
- TensorFlow
- Vitis AI
- FFmpeg
- Vitis Video
- Partners
  - Genomics,
  - Data Analytics,
  - And more

Edge Deployment
On-Premise Deployment
Cloud Deployment

© 2020 Xilinx
Anatomy of an Accelerated Application

CPU

Host Application

XRT/OpenCL API

XRT

Drivers

FPGA

Accelerated Functions

AXI Interfaces

Global Memory

DMA Engine

AXI (or PCIe)
Development is performed in the context of a platform

- A pre-configured system containing I/O, status monitoring, and lifecycle management

Standardized interfaces allow for automated composition of user functionality
Vitis: Comprehensive Development Tool Suite
Xilinx Runtime (XRT)

> **Platform- and OS-independent APIs for**
  >> Device management
  >> Memory management and data transfers
  >> Accelerator execution management

> **OpenCL wrappers, media frameworks, and domain-specific APIs built on top of base APIs**

> Open source and available on GitHub
Open Source, Standards Based Libraries

**Domain-Specific Libraries**
- Vision & Image
- Finance
- Data Analytics & Database
- Data Compression
- Data Security

**Common Libraries**
- Math
- Linear Algebra
- Statistics
- DSP
- Data Management

400+ functions across multiple libraries for performance-optimized out-of-the-box acceleration


© 2020 Xilinx
# Vitis Vision Libraries

<table>
<thead>
<tr>
<th>Module</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ISPs</strong></td>
<td>• Debayer, Auto White Balance, …</td>
</tr>
<tr>
<td><strong>ML pre/post processing</strong></td>
<td>• Resize, Letterbox, Crop, Color Conversion,…</td>
</tr>
<tr>
<td><strong>Smoothing filters</strong></td>
<td>• Bilateral, Gaussian, Median, Box,…</td>
</tr>
<tr>
<td><strong>Edge Detection</strong></td>
<td>• Canny, Gaussian of difference, Sobel,…</td>
</tr>
<tr>
<td><strong>Thresholding</strong></td>
<td>• Binary, Binary Inverse, Color, OTSU,…</td>
</tr>
<tr>
<td><strong>Morphology</strong></td>
<td>• Dilate, Erode, Houghlines, Standard Deviation,…</td>
</tr>
<tr>
<td><strong>Geotransform</strong></td>
<td>• Affine, perspective, pyrups, pyrdown, remap, translation, …</td>
</tr>
<tr>
<td><strong>Feature Detector, Descriptors</strong></td>
<td>• Fast, Harris, Histogram of Gradients ….</td>
</tr>
<tr>
<td><strong>Stereo</strong></td>
<td>• Local Block Matching, Rectify, …</td>
</tr>
<tr>
<td><strong>Tracking</strong></td>
<td>• Dense Optical Flow (LK), Extended Kalman Filter,…</td>
</tr>
</tbody>
</table>

![Color Conversion Speed Up](image1)

![Optical Flow and SGBM Speedup](image2)
Deploy: Embedded, Single Server, Scale-out

Executable

Edge Deployment

Single Server

Runtime

Scale Out

Xilinx Docker Registry

Kubernetes

Kubernetes plugin and single node resource manager
Vitis AI: Real Time AI Inference Acceleration

**Frameworks**

- TensorFlow
- Caffe
- PyTorch

**Vitis AI Models**

- AI Optimizer
- AI Quantizer
- AI Compiler
- AI Profiler

**Vitis AI Development Kit**

- 60+ pretrained, optimized reference models
- Performance improvement up to 10-20x
- Tensor based ISA for true software programmability

**DSA**

- CNN DPU
- LSTM DPU
- MLP DPU

DSA – Domain Specific Architecture
DPU – DNN Processing Unit

© 2020 Xilinx
AI Embedded in Apps, Rarely the Whole App
Example: Whole Application Acceleration

Implemented either in FPGA or CPU
Always in FPGA

2-3 days to integrate and test using Vitis and Vitis+AI Libraries

Speedup over CPU

- Tiny Yolo v3
- Resnet-50
- GoogleNet

Frames/sec

CPU
FPGA
Example: Defect Detection
Low Latency: End-to-end < 250ms

Display Output
1. Grading Results
2. Color Image
3. Binary Filling Image
4. Contour Image
Putting it All Together

AI and Data Scientists (iterations in minutes)

Application Software Developers

Embedded Developers

Hardware Developers

© 2020 Xilinx
Summary

- **Unified Software Platform**
  - Cloud to edge, software and AI
  - Comprehensive tools, runtime, libraries and models

- **Standards, Open Source**
  - Participating in open source
  - Use of standard environments & APIs
Please visit the following sites for more information

Vitis Unified SW Platform


Vitis Libraries


• [https://github.com/Xilinx/Vitis_Libraries/](https://github.com/Xilinx/Vitis_Libraries/)

Vitis AI


Visit the Avnet-Xilinx booth to see the following demonstrations in action:

• Face Detection, Pedestrian Detection, Pose Estimation, Machine Learning and more

• Hardware families include the Zynq Ultrascale+ and Versal AI Core

• Demonstration platforms include our SmartCamera+, Ultra96, and UltraZed

• Xilinx and Avnet staff will be available to answer any questions

2020 Embedded Vision Summit

• Vitis and Vitis AI: Application Acceleration from Cloud to Edge

• September 17, 2020, 11:00-11:30AM PDT