

**Enabling Small Form Factor, Anti-Tamper, High-Reliability,
Fan-less Artificial Intelligence and Machine Learning**



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE

Smart Embedded Vision Today

Accelerate Smart Embedded Vision at the Edge Supporting 4K Resolutions with Low-Power 12.7 Gbps SERDES



- **Different application use cases with common requirements**

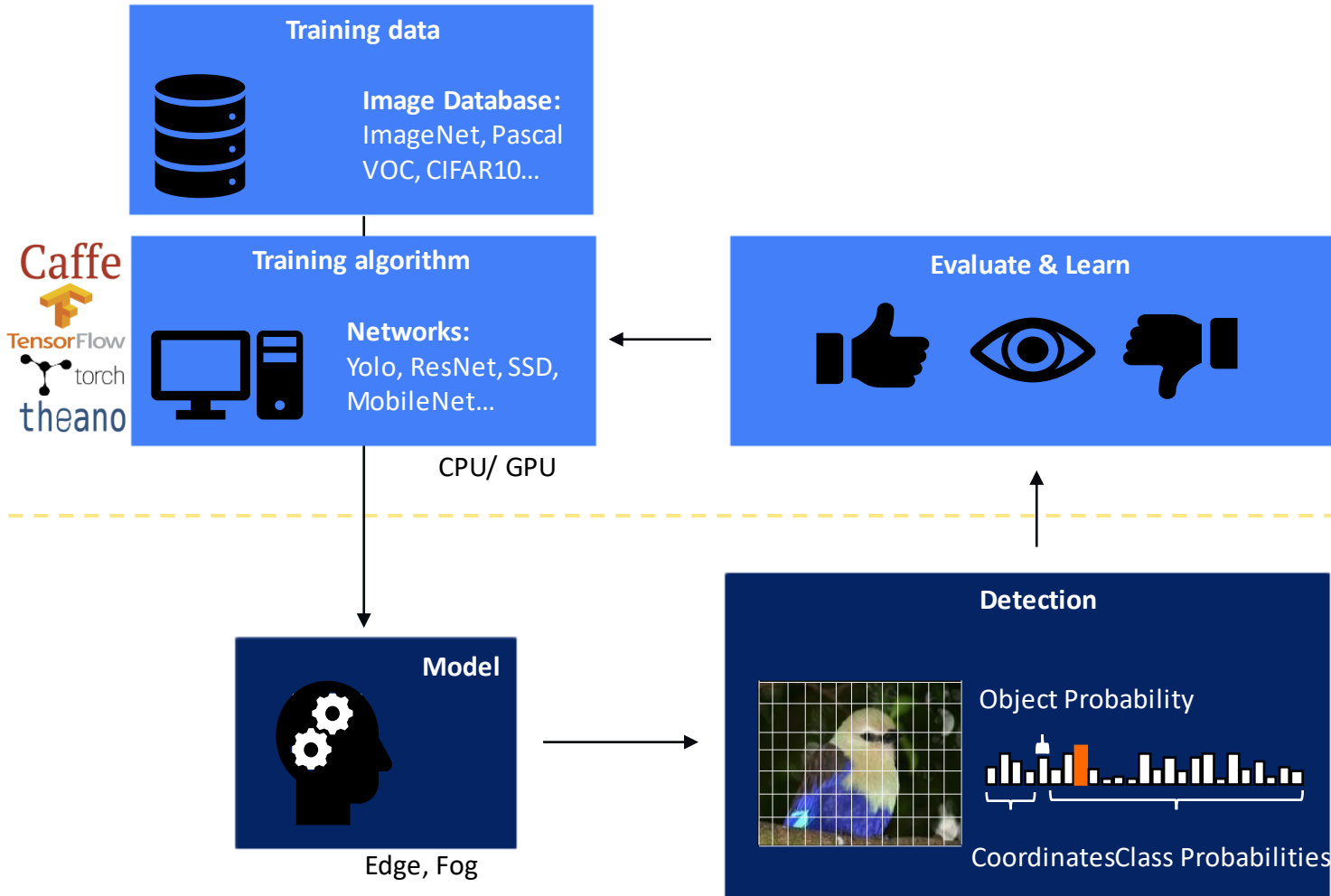
- More pixels 1080p moving towards 4K/8K
- Small form factor Not enough space to fit a heat sink and thermal fan
- More secure Ensure safe operation and protection against tamper

Our Objective Today



Low-power, Fan-less, Artificial Intelligence (AI) Camera for the Edge

The Deep Learning Construct



Network Training

- In the data centre or workstation
- Large compute capacity
- No power or space constraints

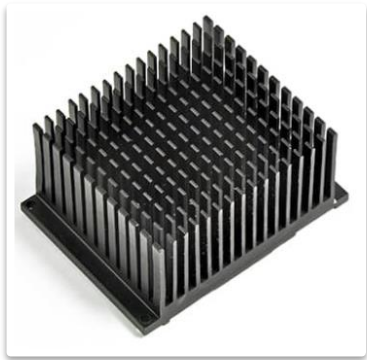
Inference

- Need low latency
- Power and space constrained
- Requires security and reliability



Design Challenges – Power

- **Implications to high power consumption**
 - Increased module size to fit heat sinks and cooling fans
 - Increased BOM
 - Increased image processing complexity to manage interference in thermal imaging
 - Decreased battery life, increased weight due to larger batteries
 - Decreased compute envelope to operate within temperature constraints



Heat sinks needed power consumption >5W

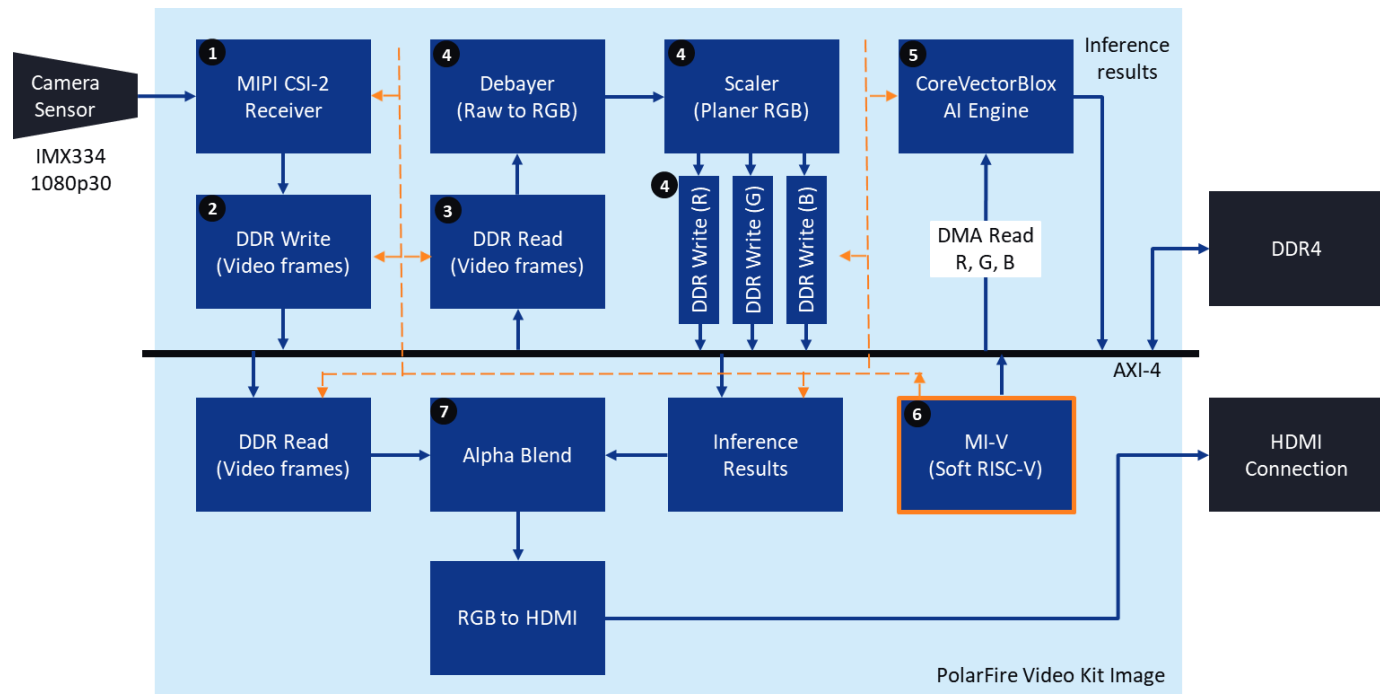


Active cooling requires fans and onboard power electronics and add up to \$10 in bill of materials (BOM)



Portable, battery-powered devices consuming more power will require heavier batteries

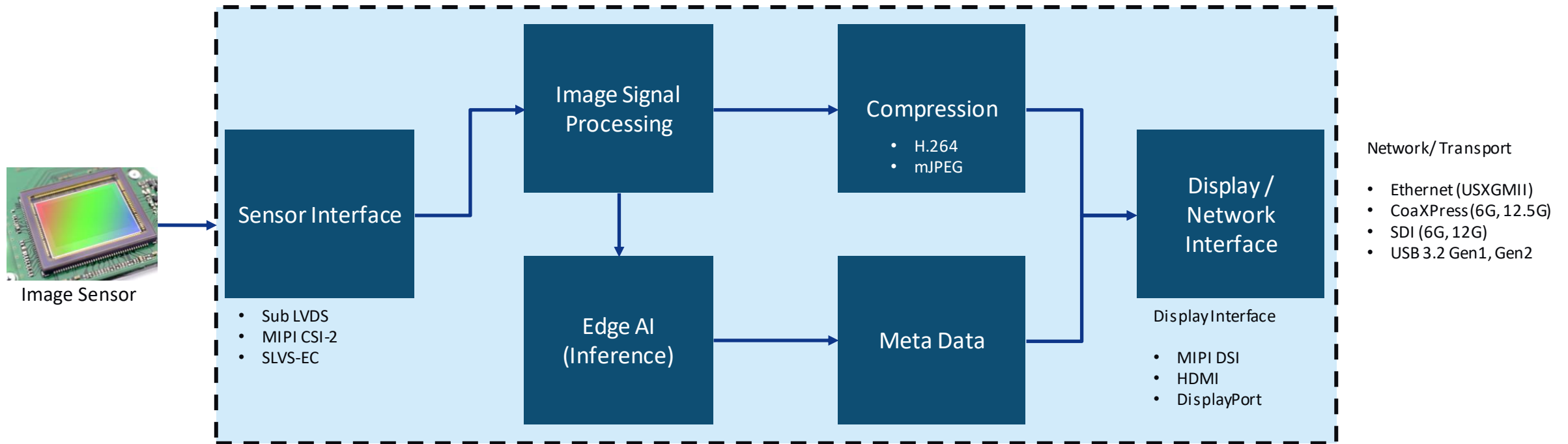
Design Challenge – Advance Driver Assistance Systems (ADAS)



- **Implications to safe and reliable operation**

- Can the design withstand, detect, correct or report errors arising out of
 - Processes, random events and transient causes
- Whether it enables safe designs as prescribed to operate in
 - Industrial applications - IEC61508
 - Automotive applications - ISO26262

Design Challenge – Evolving Requirements

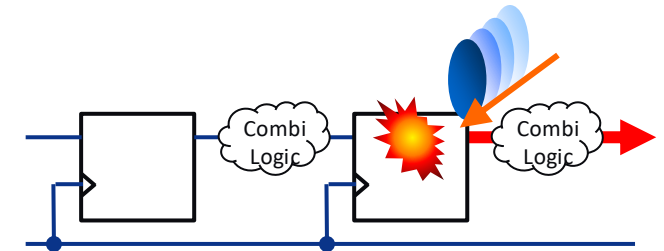


- **Requirements for Embedded Vision**

- Newer AI algorithms, more frameworks
- Different sensor interfaces, In-System Programming (ISP), compression techniques, network interfaces

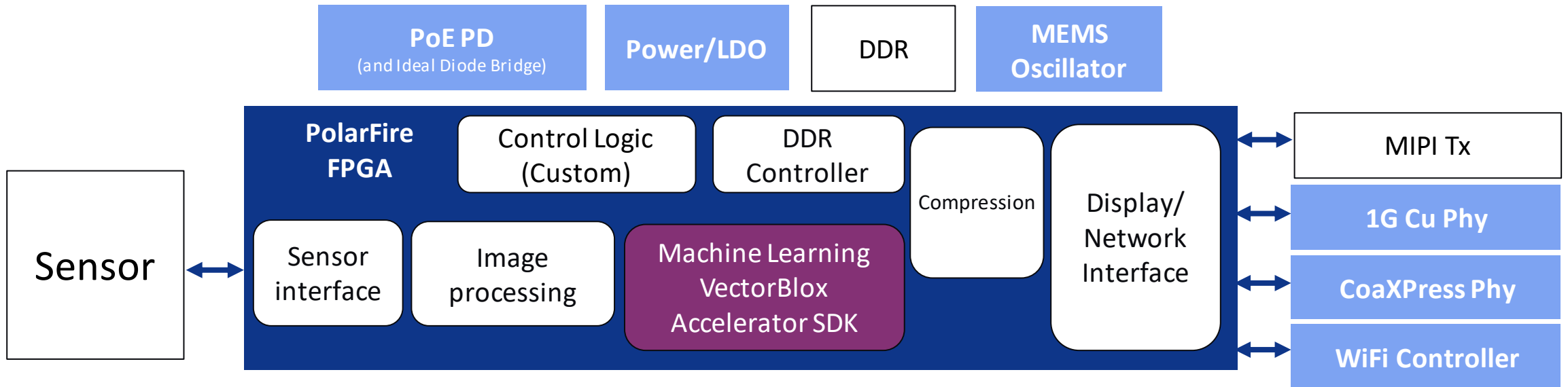
Design Challenge – Reliability

- **Volumes and deployment locations demand reliability**
- **Single Event Upsets (SEU) due to Soft-Errors**
 - Caused due to high-energy particle strikes
 - Prevalent in Space and Avionics levels
 - **Also, at the ground level**
 - Neutrons generated in Earth's atmosphere
 - Alpha particles generated by radioactive isotopes in package materials
- **Implications due to SEU lead to catastrophic system failure**
 - SEU on a data bit in flip-flop can introduce logic errors
 - Corrupt bit in data memory may be read multiple times
 - Configuration error in programmable logic changes functionality



A0	A1	A2	A3	A4	A5	A6	A7
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7
D0	D1	D2	D3	D4	D5	D6	D7
E0	E1	E2	E3	E4	E5	E6	E7
F0	F1	F2	F3	F4	F5	F6	F7
G0	G1	G2	G3	G4	G5	G6	G7
H0	H1	H2	H3	H4	H5	H6	H7

Using FPGAs for AI and Embedded Vision



- **Sensor Interfaces (Rx)**

- MIPI CSI-2
- SLVS-EC v1.2 & v2.0

- **Compression**

- H.264 encode
- mJPEG

- **Image Processing**

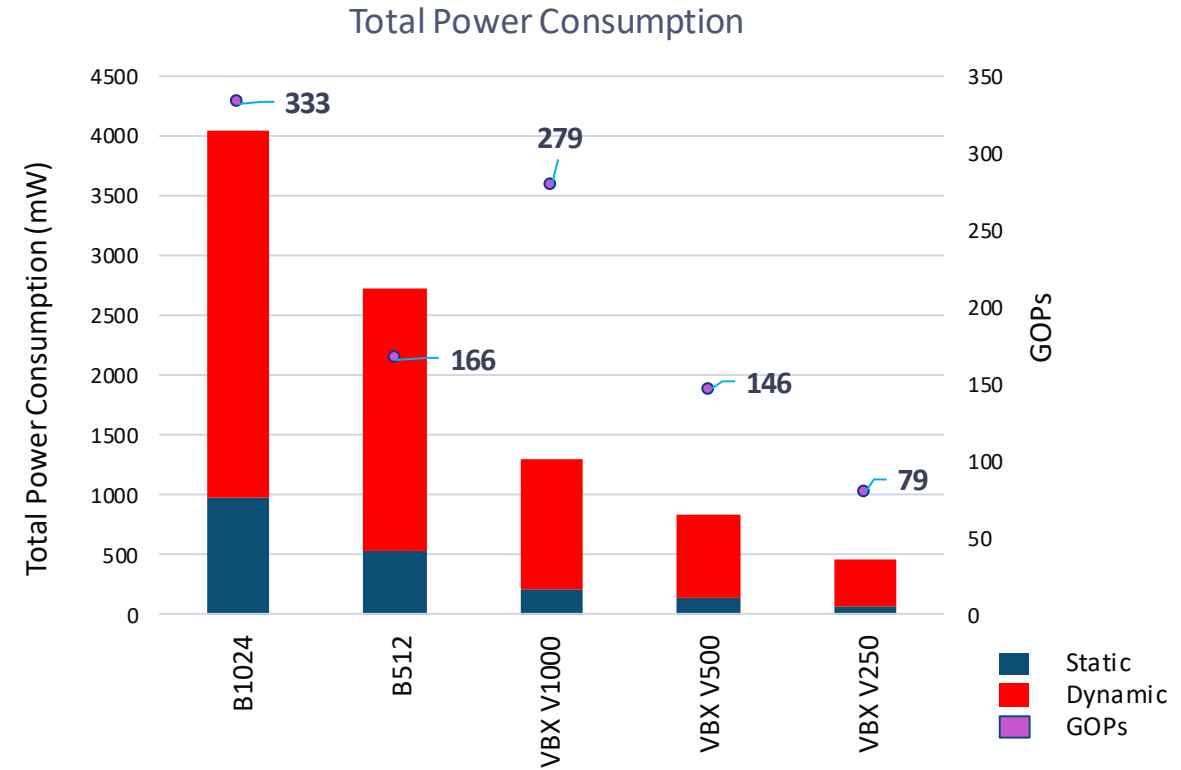
- Alpha blending
- Bayer interpolation
- Image edge detection
- Image sharpen
- RGB to YCbCr
- YCbCr to RGB
- Histogram
- White balance
- Gamma correction

- **Transport Interfaces**

- CoaXPress[®] 12G
- SDI 12G
- 10G MAC / 10G PHY
- USXGMII 1, 2.5, 5, 10G
- HDMI 2.0
- DisplayPort 1.4a
- USB 2.0, USB 3.2 Gen1/2
- 10 GigE Vision

Microchip FPGAs Deliver Fan-less Edge Compute

Core Name	Peak GOPs	Dynamic Power (mW)	Static Power* (mW)	Total Power (mW)	Total Power (mW/GOP)
VectorBlox V1000	279	1094	206	1300	5.1
VectorBlox V500	146	698	127	825	6.4
VectorBlox V250	79	387	65	452	7.1
Comp A B1024	332.8	3072	976	4048	12.2
Comp A B512	166.4	2201	528	2729	16.4

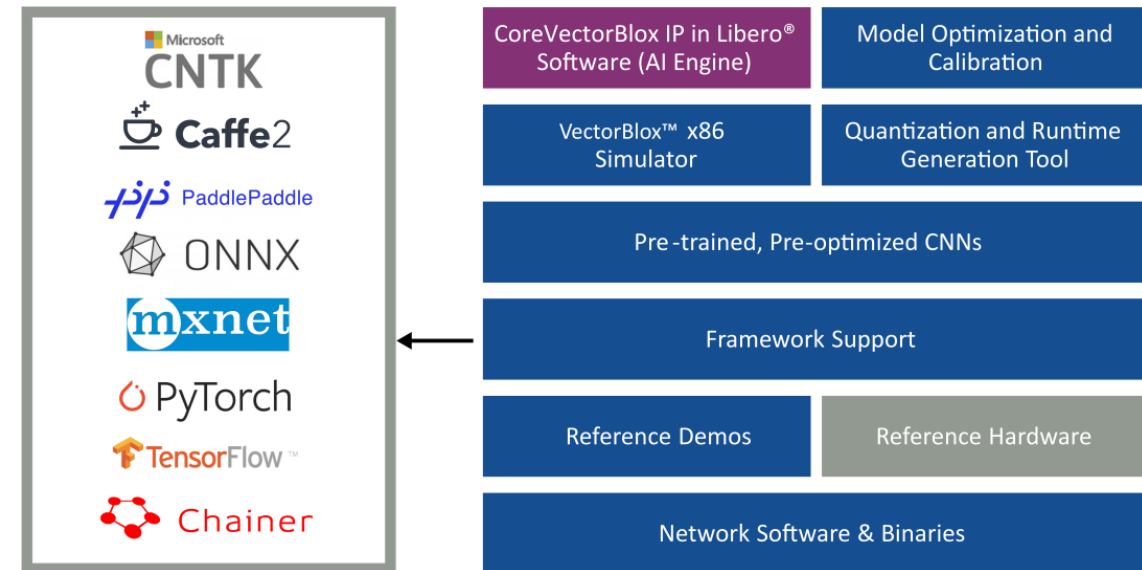


- **2-3x more power efficient inferencing for similar performance output**
- **Suitable for applications requiring**
 - Low power consumption, small enclosures and fan less designs

*Scaled for resource utilization

VectorBlox™ Software Development Kit (SDK) for Microchip FPGAs

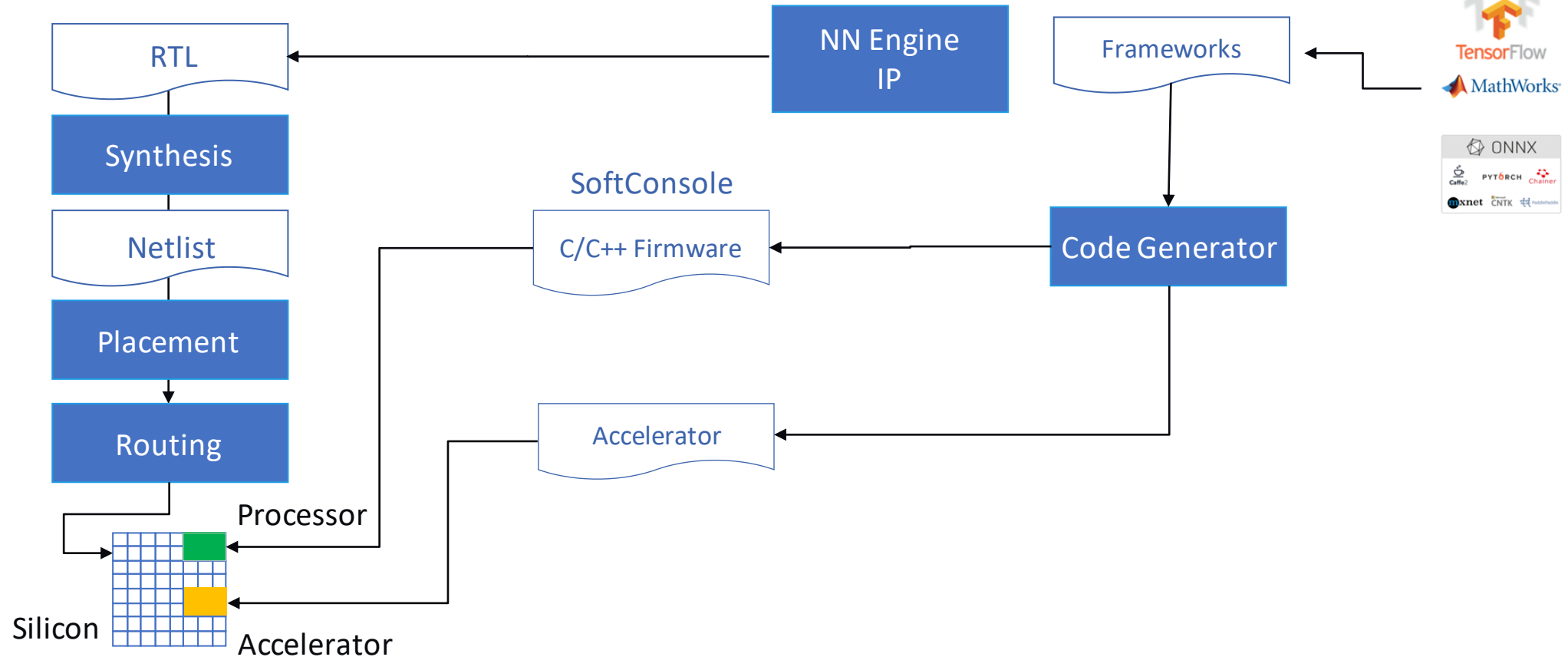
- Enables developers to code in C/C++ and use power-efficient neural networks for inference
 - No prior FPGA design experience required
- Accepts models in TensorFlow, ONNX, etc.
 - Offers the widest framework interoperability
- Includes a bit accurate simulator
 - Validate CNN in software environment
- Pre-trained neural networks demos included
 - Load network models at run time on supported hardware



Software Abstraction for Neural Networks

Traditional FPGA Flow

VectorBlox™ Accelerator
SDK



Power Estimation Example: Facial Recognition

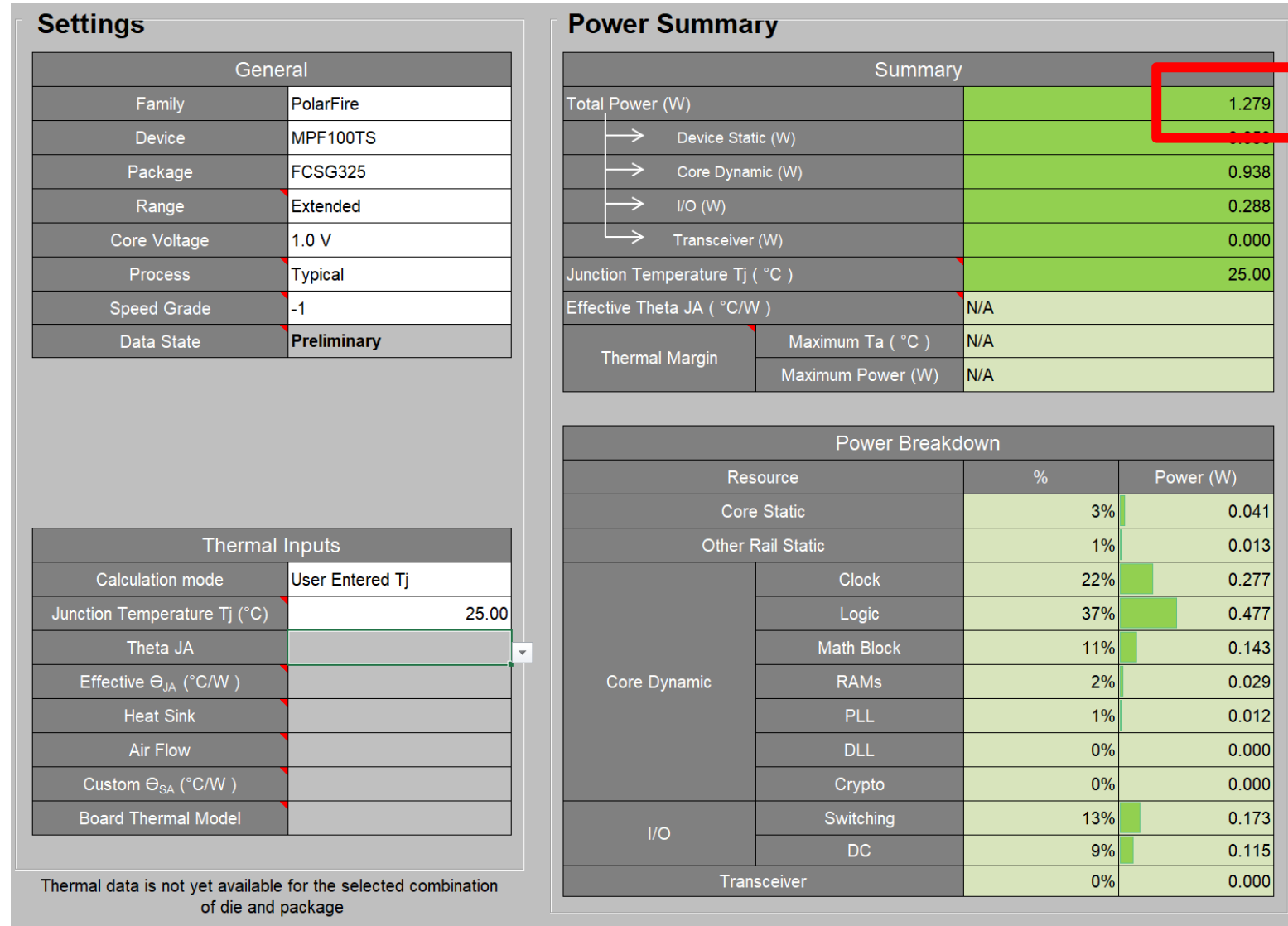
- **A two-step process, 2 Convolutional Neural Networks (CNN) with one Accelerator**
- **First BlazeFace**
 - Used in mobile apps
 - 3.8GOPs with 6M parameters (estimated)
 - Multi outputs
 - Bounding box
 - Eyes, nose, mouth, ears
 - Confidence value
- **Second SphereFace**
 - 3.5GOPs with 22M parameters
 - Runs on each face detected by BlazeFace
 - Input 112x96 image (produced from BlazeFace bounding box)
 - Output is a 512 element vector
 - 512 vectors are compared to the vector of known faces
 - Person of interest photo is run through SphereFace to build a known face vector



Power Analysis

Design includes

- V250
- Mi-V (AXI4)
- LSRAM
- AXI4 interconnect
- SPI controller
- Image scaler
- DDR4 controller



What is Available Today

- **SDK in GitHub**

- Tools

- Model Optimization
 - Calibration
 - Simulator

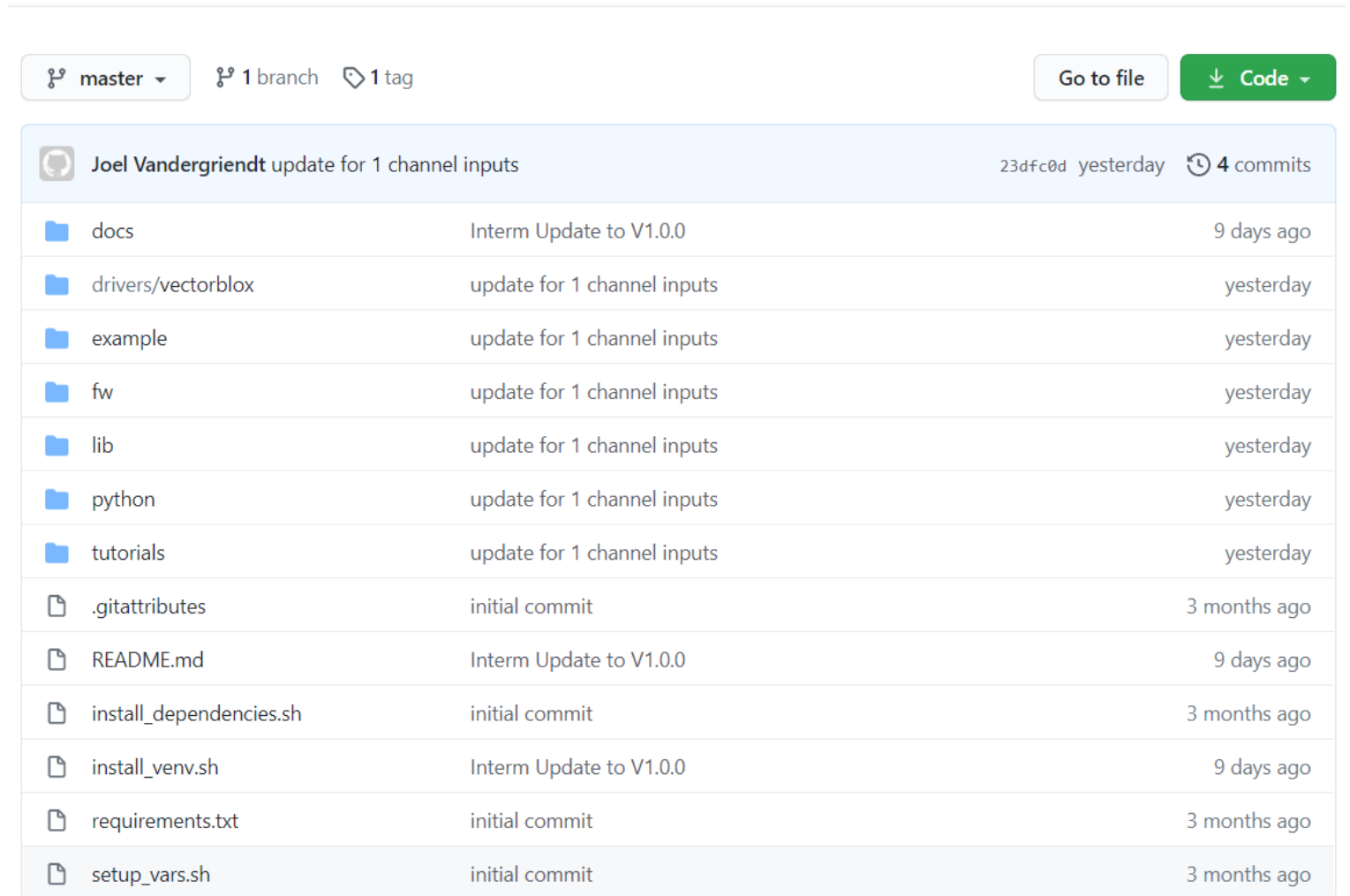
- Tutorials

- Documentation

- **VectorBlox Website**

- Hardware

- Example Projects



The screenshot shows a GitHub repository page for the commit 'Joel Vanderriendt update for 1 channel inputs' (23dfc0d, yesterday, 4 commits). The repository is on the 'master' branch, has 1 branch, and 1 tag. A 'Go to file' button and a 'Code' button are visible. The file list includes folders like 'docs', 'drivers/vectorblox', 'example', 'fw', 'lib', 'python', and 'tutorials', and files like '.gitattributes', 'README.md', 'install_dependencies.sh', 'install_venv.sh', 'requirements.txt', and 'setup_vars.sh'. The commit history for each file is shown, with most files having an 'initial commit' 3 months ago, and some having an 'Interim Update to V1.0.0' 9 days ago.

File/Folder	Commit Message	Commit Date
docs	Interim Update to V1.0.0	9 days ago
drivers/vectorblox	update for 1 channel inputs	yesterday
example	update for 1 channel inputs	yesterday
fw	update for 1 channel inputs	yesterday
lib	update for 1 channel inputs	yesterday
python	update for 1 channel inputs	yesterday
tutorials	update for 1 channel inputs	yesterday
.gitattributes	initial commit	3 months ago
README.md	Interim Update to V1.0.0	9 days ago
install_dependencies.sh	initial commit	3 months ago
install_venv.sh	Interim Update to V1.0.0	9 days ago
requirements.txt	initial commit	3 months ago
setup_vars.sh	initial commit	3 months ago

<https://github.com/Microchip-Vectorblox/VectorBlox-SDK>

http://www.microchip.com/fpga_VectorBlox

Thank you!

Empowering Product Creators to Harness Edge AI and Vision



The Edge AI and Vision Alliance (www.edge-ai-vision.com) is a partnership of >100 leading edge AI and vision technology and services suppliers, and solutions providers

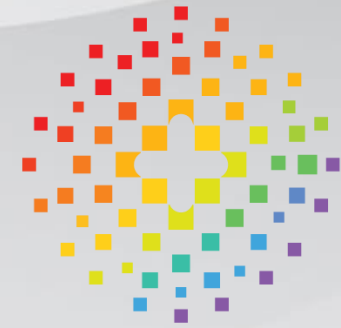
Mission: To inspire and empower engineers to design products that perceive and understand.

The Alliance provides low-cost, high-quality technical educational resources for product developers

Register for updates at www.edge-ai-vision.com

The Alliance enables edge AI and vision technology providers to grow their businesses through leads, partnerships, and insights

For membership, email us: membership@edge-ai-vision.com



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- *“Awesome! I was very inspired!”*
- *“Fantastic. Learned a lot and met great people.”*
- *“Wonderful speakers and informative exhibits!”*

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- High-quality, practical **technical, business and product talks**
- Exciting **demos, tutorials** and **expert bars** of the latest applications and technologies

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