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NeuPro-M: Highly Scalable, Heterogeneous and Secure Processor for High-Performance AI/ML in Smart Edge Devices

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AI Technology Challenges



Performance – ML prevails alternatives: More use-cases → More sensors → More pixels → More data





Scalability – Different use-cases, different needs: ADAS, Autonomous L1-L5, Powertrain, Infotainment, DMS/OMS, ...





Low power – Constrained energy envelope



Flexibility – Technology evolution faster than product deployment



Riskless & Fast Solution – Software abstraction + hardware agnostic <u>comprehensive and compatible software is key</u>



CEVA's Approach



Performance Optimized	 Heterogenous, parallel multi-element compute engine Wide range, mixed precision support 	5
Aggressive Bandwidth Reduction	 Latency optimized via hierarchical memory structure Lossless compression, on-the-fly sparsity 	5.7
Multiple Use-Cases	 Scalable and secure multi-engine, multi-core solution Automotive ISO26262 safety compliant 	57
Long Term Solution	 Innovative next-gen NN heterogeneous compute architecture Vector Processing Unit in every engine enables flexibility 	5
Fast, Simple & Riskless Implementation	 Comprehensive, system level toolchain, utilizes HW capabilities Supports open source languages and frameworks 	5



NeuPro-M At-A-Glance







NeuPro-M Block Diagram





10 Top Distinctive NeuPro-M Features



NeuPro-M Feature List Highlights	Low Power	High Utilization	High Performance	Low Bandwidth	Low Latency	Agility / Scalability
Ultimate Control Scheme	<	<	×	<	<	<
Out-of-the-box Winograd transform	\checkmark	\checkmark	\checkmark			
True (unstructured) Sparsity	<	<	<	\checkmark		
Unique GRID micro architecture [Activation x Weights] (data type diversity with minimal power consumption)	\checkmark	\checkmark	<	<		<
Programmability		\checkmark	×	\checkmark		<
Optimized (reduced) Data Traffic	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	
Data Compression	<			\checkmark	\checkmark	
Next Generation Al Features (e.g. transformers, 3D convolution)		\checkmark	\checkmark			<
Matrix Decomposition	<	\checkmark	×	\checkmark	\checkmark	
Safety / Security						\checkmark



Out-of-the-box (untrained) Winograd Transform

- Alternative efficient way performing convolution
 - Using <u>half</u> the MACs (Multiply And Accumulate) operations
 - Reduced power consumption
 - Negligible precision degradation
- 2x performance gain for 3x3 convolution layers
- Out-of-the-box Winograd "convolution"
 - Untrained = <u>No dedicated retraining needed</u>
 - 8-bit with <0.5% precision degradation</p>
 - Wide range of data types supported
 - 4-bit, 8-bit, 12-bit, 16-bit





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NeuPro-M

True Sparsity: Unstructured Pruning



Ability to "skip" zeros in data/activations or weights along inference process

Performance gain by avoiding multiplication by zeros

- Up to 4x performance gain
 - Bandwidth reduction
 - Power reduction
- Preserves accuracy
- Full HW & SW support
 - Training for data optional
- Unstructured sparsity
 - Essential for data
 - ▷ Higher weights sparsity level



gain on most use-cases



Data Type Diversity / Flexibility



- Various data types support with minimal power 2-bit
 Low bit data and weights will generate
 Lower bandwidth
 Reduced power consumption
 Performance acceleration
 Different layers using different data/weights types, while overall precision kept
- Flexibility tackles different use cases

Туре		[bit]	х	[bit]	# of MACs	
2 hit		254	2	х	2	6.0 K
Z- DIL		ary	8	x	2	4.0 K
			4	x	4	16.0 K
1 hit	Eived	noint	4	x	8	8.0 K
4-bit Fixed	Fixed	point	4	x	12	5.3 K
			x	16	4.0 K	
	8-bit Fixed		8	x	8	4.0 K / 8.0 K*
8- bit		point	8	x	12	2.7 K / 4.0 K*
				x	16	2.0 K / 4.0 K*
17 hit	12 bit Fixed point		12	x	12	1.8 K / 2.3 K*
	Fixed	* With 50% sparsi	ty 12	x	16	1.3 K / 2.0 K*
16- bit	bit Fixed point		16	x	16	1.0 K / 2.0 K*
16- bit	Half precision	Floating-point	16	x	16	64
32- bit	Single precision	Floating-point	32	х	32	32



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Single Engine NeuPro-M Core Performance





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Ultimate Control Scheme

- Unique, optimized and interleaved control scheme
 - Mixture of software & hardware operations, orchestrates heterogenous hardware
 - Engines, co-processors, local controllers, DMAs & queue managers
 - Ensures efficient and deterministic performance
 - Optimal parallel interleaved operation
- No need to redispatch program upon layers
 - Reduces system data traffic and software complexity
- On the fly, 'head to tail' fused operation pipeline
 - Hardware based task flow control (not software interrupt based)
 - <u>Reduces</u> internal & external memory access e.g. L1, L2, DSP, DDR



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Example of "on-the-fly" fused operations



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NeuPro-M Comprehensive Toolchain





CDNN Supports Open-Source Ecosystem







NeuPro-M: Optimized AI Solution in Every Layer





Data & Weights

Mixed Precision: 32/16/12/8/4/2 bits, Fixed-point, Single/Half precision floating-point, Sparsity

W

Elementary Operation

Winograd, Transformers, 3D-Convolution, Programmable operation, Depthwise-Convolution

Reduced Data Traffic

Bandwidth, Latency, Memory hierarchy, Data/Weights compression, Realtime clients

System & Flow Control

Compound parallel processing, Metrix decomposition, Decentralized data management

Neural Network Models

HW-aware networks, CDNN Compiler, CDNN-Invite, Asymmetric quantization, Pruning



NeuPro-M[™] – Heterogeneous and Secure High Performance Al/ML Architecture for Smart Edge Devices



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- NeuPro-M Overview: <u>https://www.ceva-dsp.com/product/ceva-neupro-m/</u>
- CDNN Compiler: <u>https://www.ceva-dsp.com/product/ceva-deep-neural-network-cdnn/</u>
- Fortrix, Root-of-Trust and Security IP: <u>https://www.ceva-dsp.com/product/fortrix-secured2d/</u>
- SensPro, Sensor-hub and Computer Vision Processor: <u>https://www.ceva-dsp.com/product/ceva-senspro/</u>





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THANK YOU

