Fast-Track Design Cycles Using Lattice's FPGAs

Hussein Osman

Marketing Director

Lattice Semiconductor

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Embedded Vision Trends

Support multiple sensors and displays

Move to higher resolutions and faster frame rates

Connect MIPI and legacy components

Enable AI processing at low power

These trends require hardware with:

- Low Power
- Small Form Factor
- High Performance
- High Reliability
- Ease of Use

Edge Processing Challenges

Edge devices typically run on battery and are thermally challenged requiring low power profile

Rapidly changing deep learning AI algorithms

Heterogenous compute is required with HW accelerators assisting CPUs

GPUs used as accelerators best when executing the same instruction in parallel, also power hungry

Getting to market quickly

Compute requirement doubling every 3 month, 7x faster than Moore's law

SoC based heterogeneous compute is rigid, the HW accelerators are not programable

Spinning new versions of ASICs and ASSPs is costly limiting the update cycle of the HW blocks

FPGA adaptable architecture is required to accelerate compute efficiently

Why FPGA for Edge AI

Ultra-low Power
1 milliwatt to 5 W power consumption

Scalable Performance To Handle Multiple Use Case
Executes multiple use cases in parallel or serial

Secure
Secure device configuration

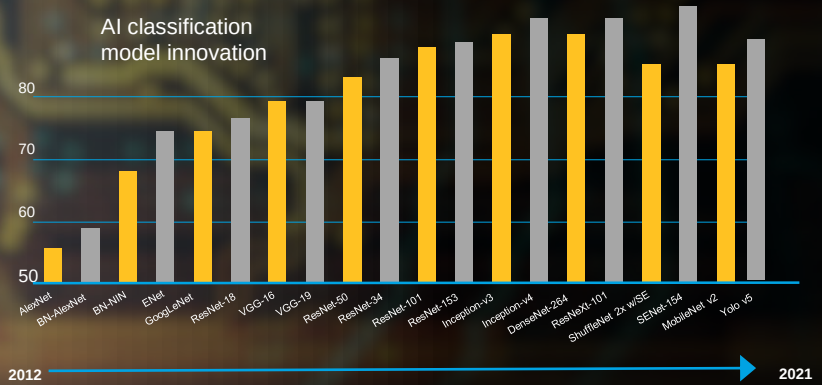
Flexible Computation Resources
Pre and post processing of data such as ISP, FFT and filtering

Hardware Programmable
Adapts to fast changing machine learning algorithms

The Speed of AI Innovation Benefits Programmable Logic to Keep Delivering the Best Experience.

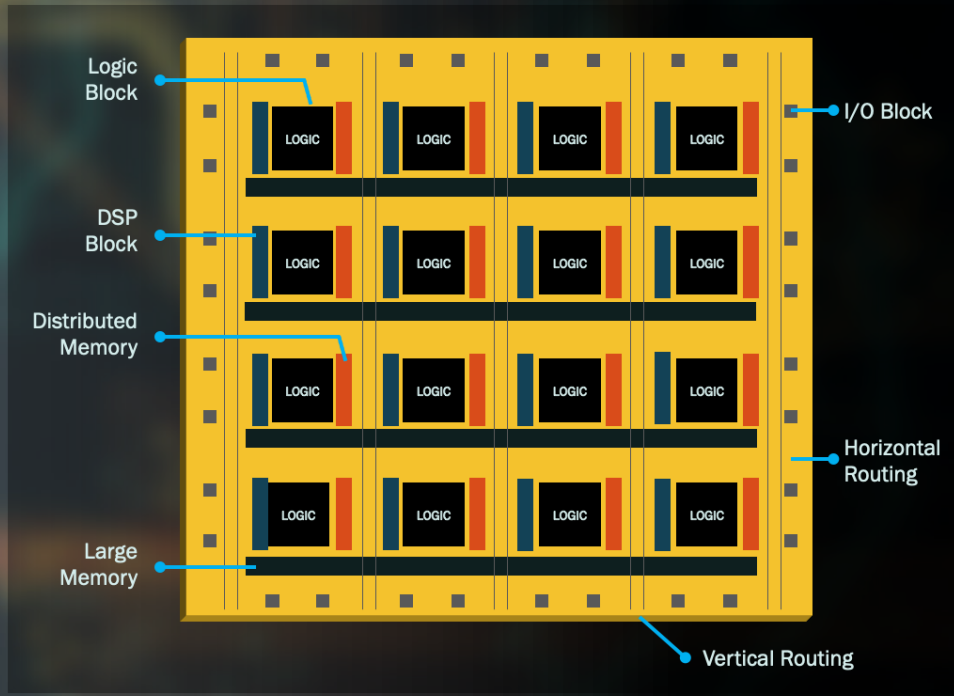
Hardware optimization & **Algorithm optimization** = **Continuous improvement and new use cases**

AI models are rapidly evolving

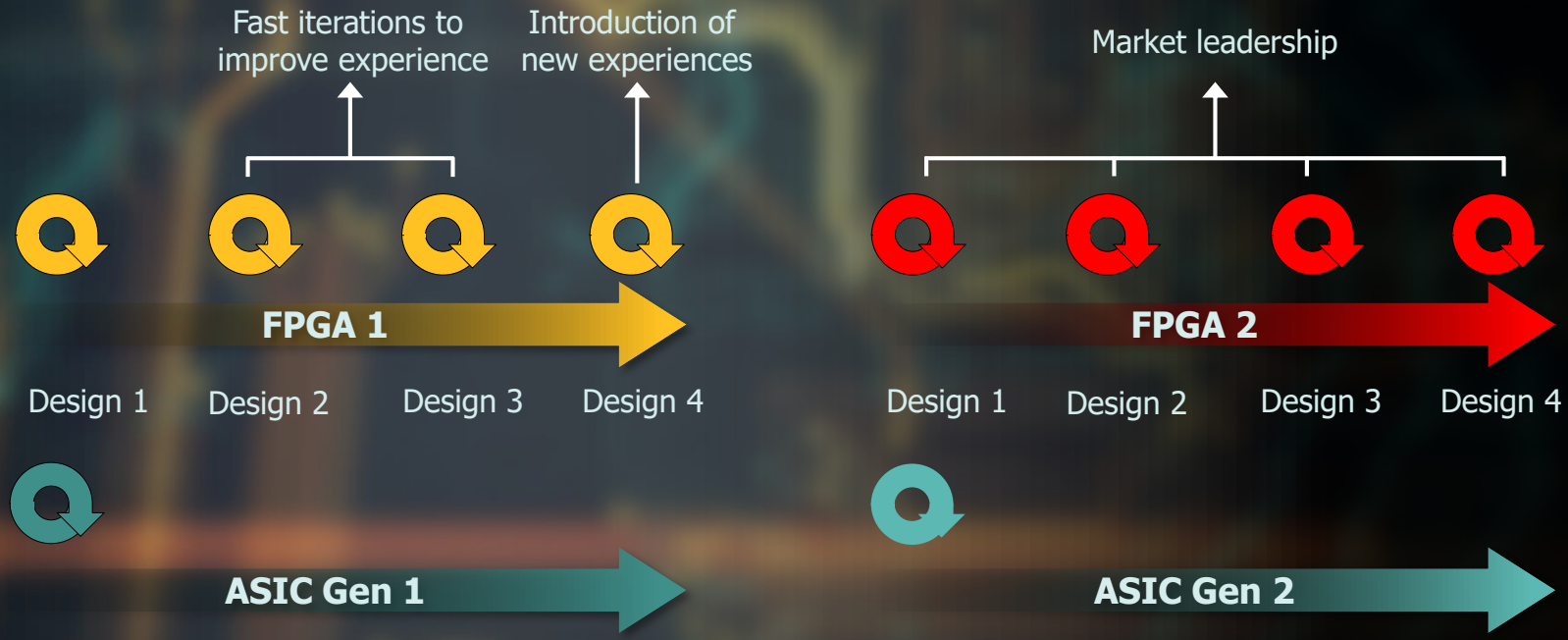


FPGA Architecture – Programable Distributed Resources

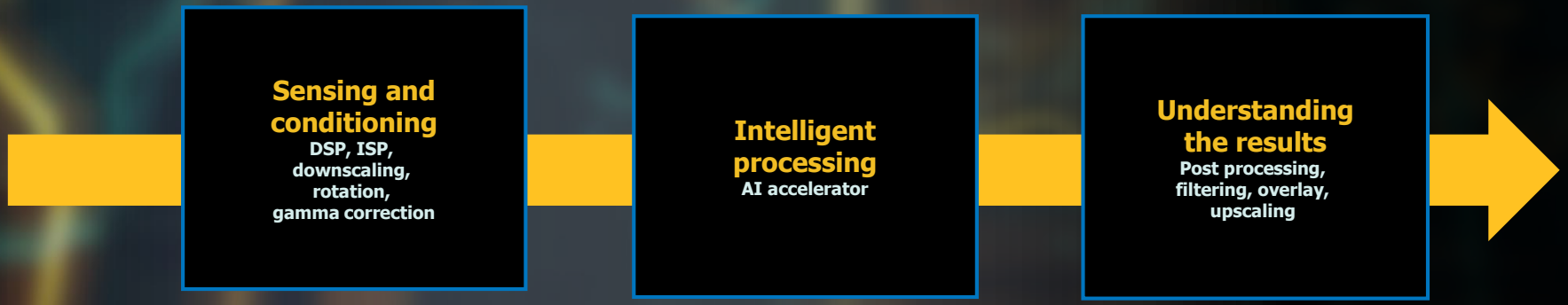
- Building blocks are distributed throughout the fabric
- Extensive interconnect routing connecting blocks
- Flexible I/Os to move data in and out
- Similar approach to modern AI ASICs



AI Models Evolve Rapidly, Requiring Agile Development Cycles that ASICs Cannot Match



Vision Pipeline: End-to-end Hardware Implementation



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CUSTOM DESIGN SERVICES

Smart Home | Smart City | Smart Factory | Smart Car | Client Compute Experiences

REFERENCE DESIGNS / DEMOS

Hand Gesture Detection | Key Phrase Detection | Human Presence Detection | Human Attention Tracking | Object Counting | Object Classification

SOFTWARE TOOLS

sensAI Studio | Neural Network Compiler

LATTICE RADIANT DESIGN SOFTWARE | LATTICE PROPEL | Caffe | TensorFlow | TensorFlow Lite | Keras | LATTICE DIAMOND DESIGN SOFTWARE | Glance

IP CORES

Neural Network Accelerators

CNN Compact Accelerator | CNN Accelerator | CNN Plus Accelerator | CNN Co-Processor Accelerator | Advanced CNN Accelerator

HARDWARE PLATFORMS

Upduino | CrossLink™-NX Voice and Vision ML Board | CertusPro™-NX Voice and Vision ML Board | ECP5™ EVDK | Avant Evaluation Board

iCE40™ UltraPlus	CrossLink™-NX	CertusPro™-NX	ECP5™	Avant™
1-20 mW, 5.5 mm²	50-200 mW, 16 mm²	400 mW, 81 mm2	250 - 850 mW, 100 mm2	1 - 5 W, 100 mm2

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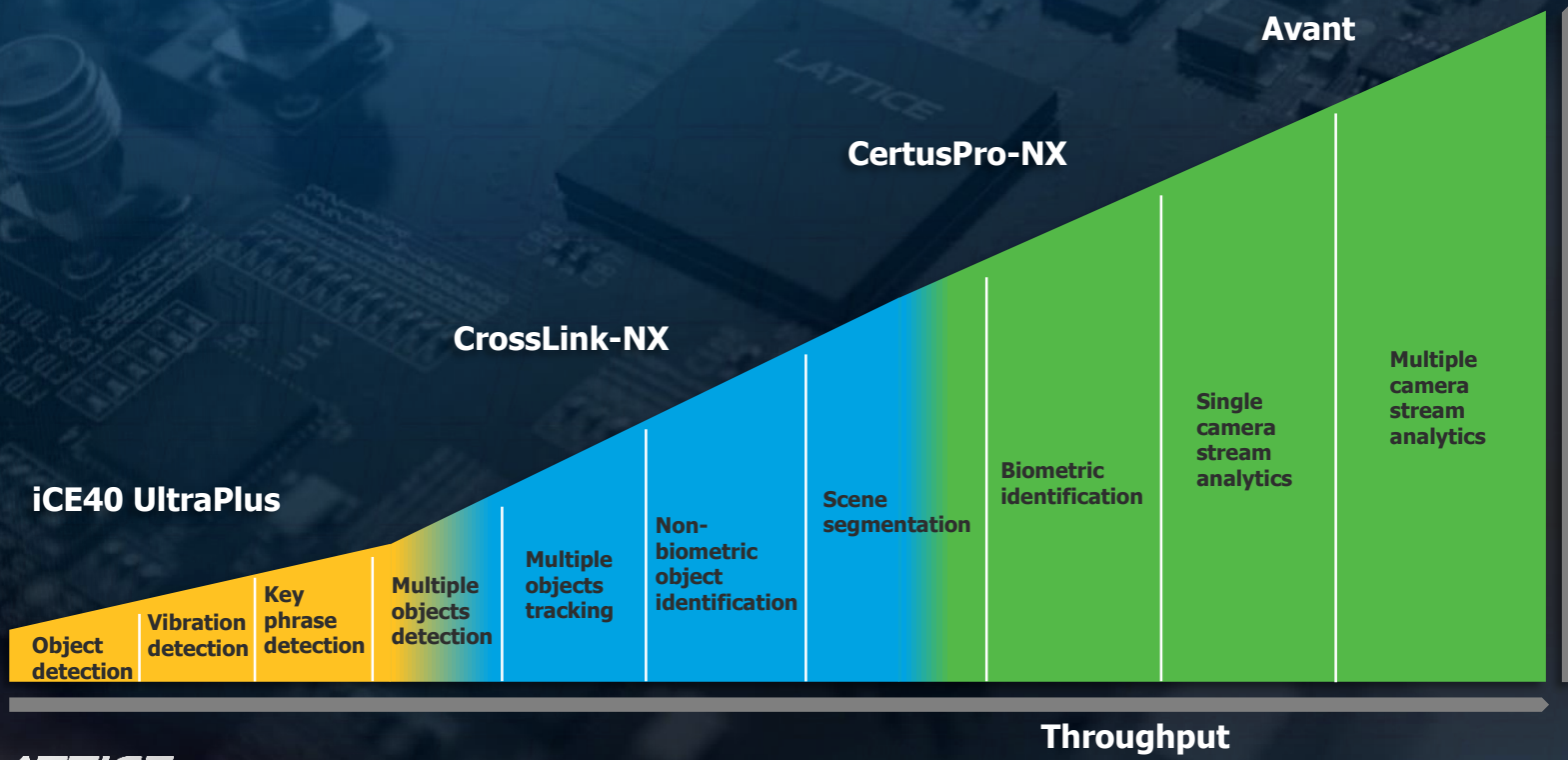
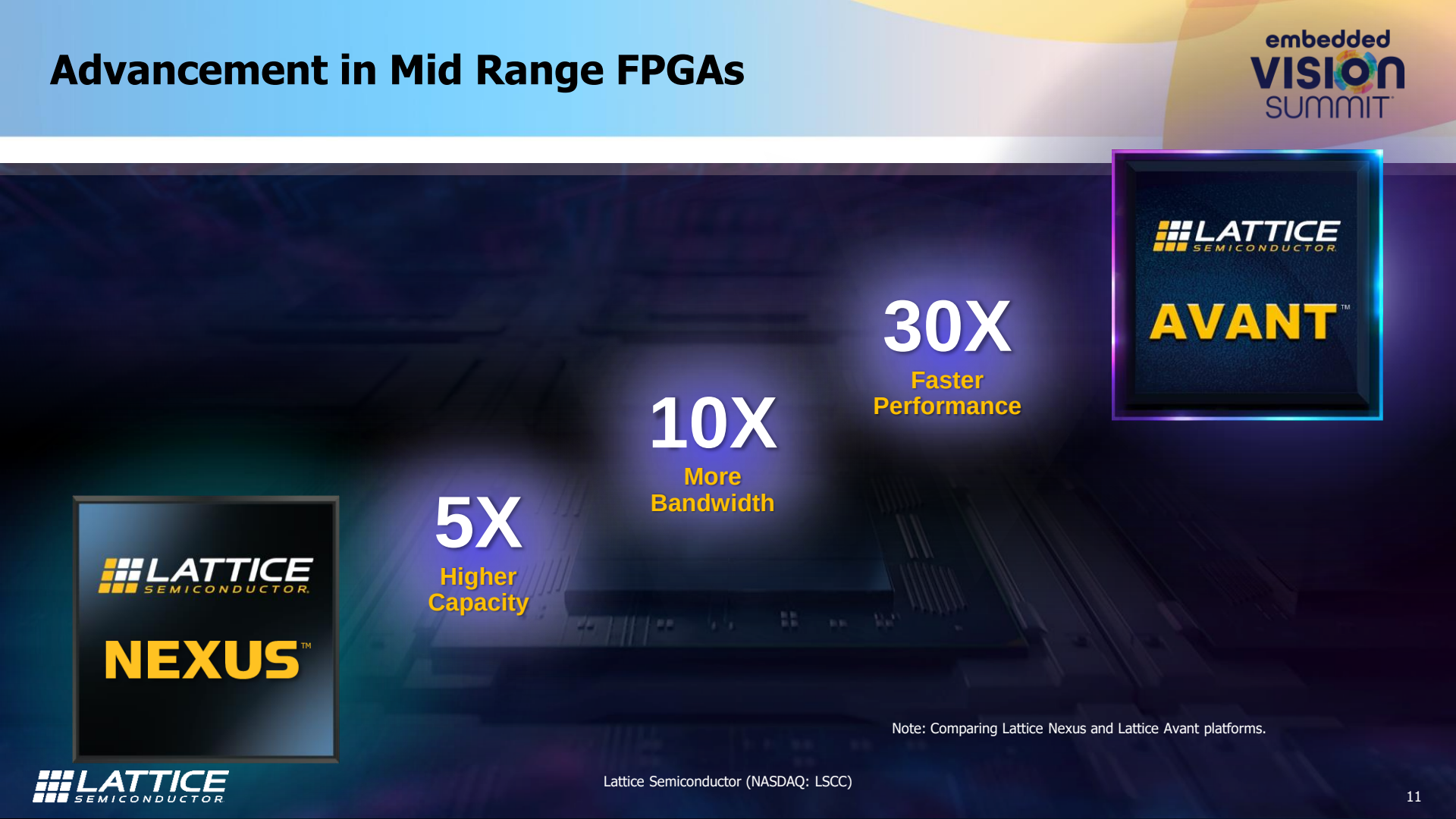
Applications Supported Across FPGAs



Advancement in Mid Range FPGAs



Note: Comparing Lattice Nexus and Lattice Avant platforms.

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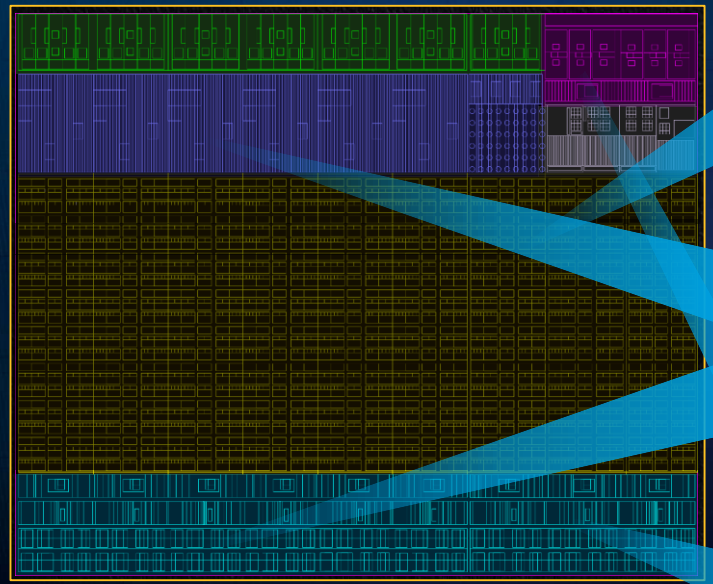


OPTIMIZED COMPUTE

- Enhanced DSP tuned for AI inferencing
- Flexible and distributed embedded memory

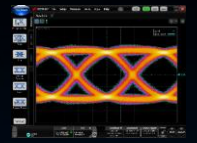
On-Chip Compute Elements

POWER EFFICIENCY

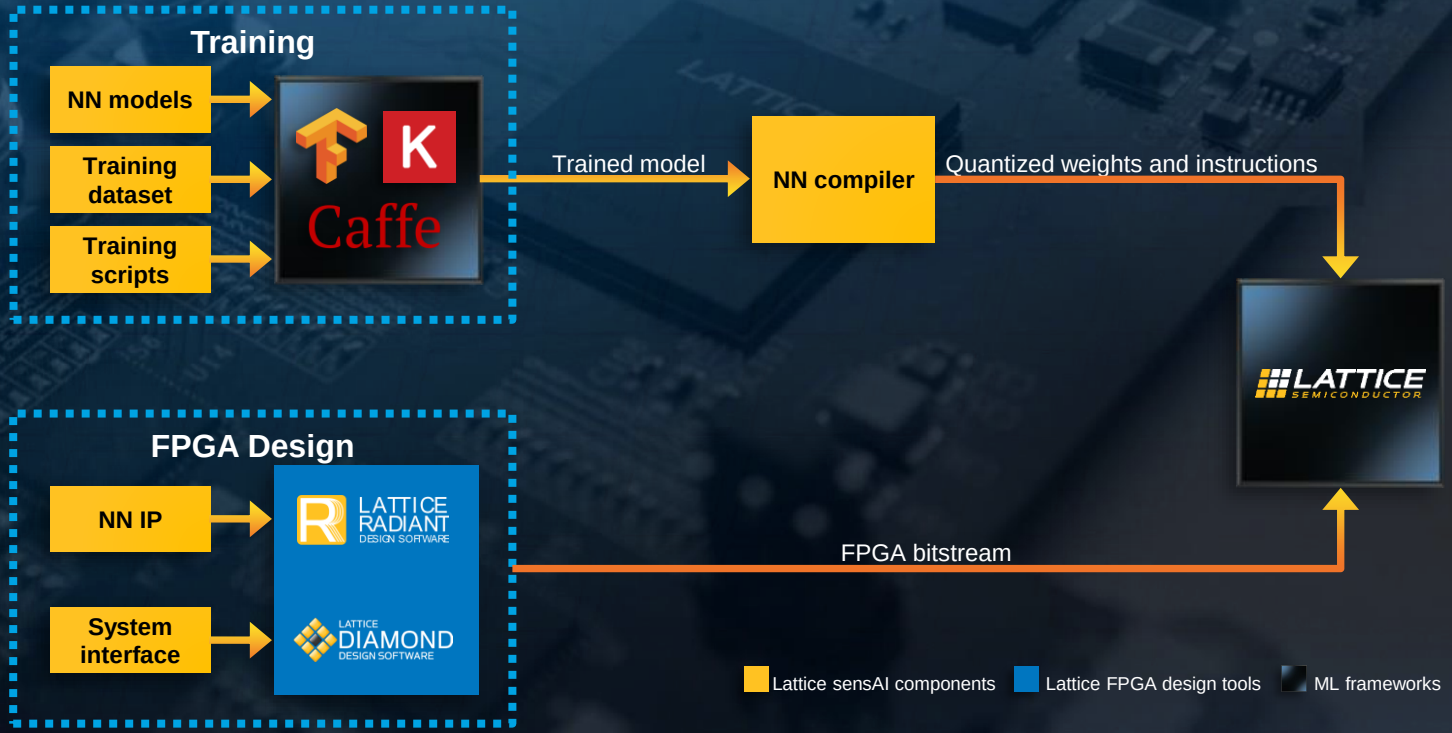
- Programmable fabric architected for low power
- Power optimized embedded memory and DSP
- Power efficient SERDES and I/O designs
- Built-in protocol logic for lower system power

ADVANCED CONNECTIVITY

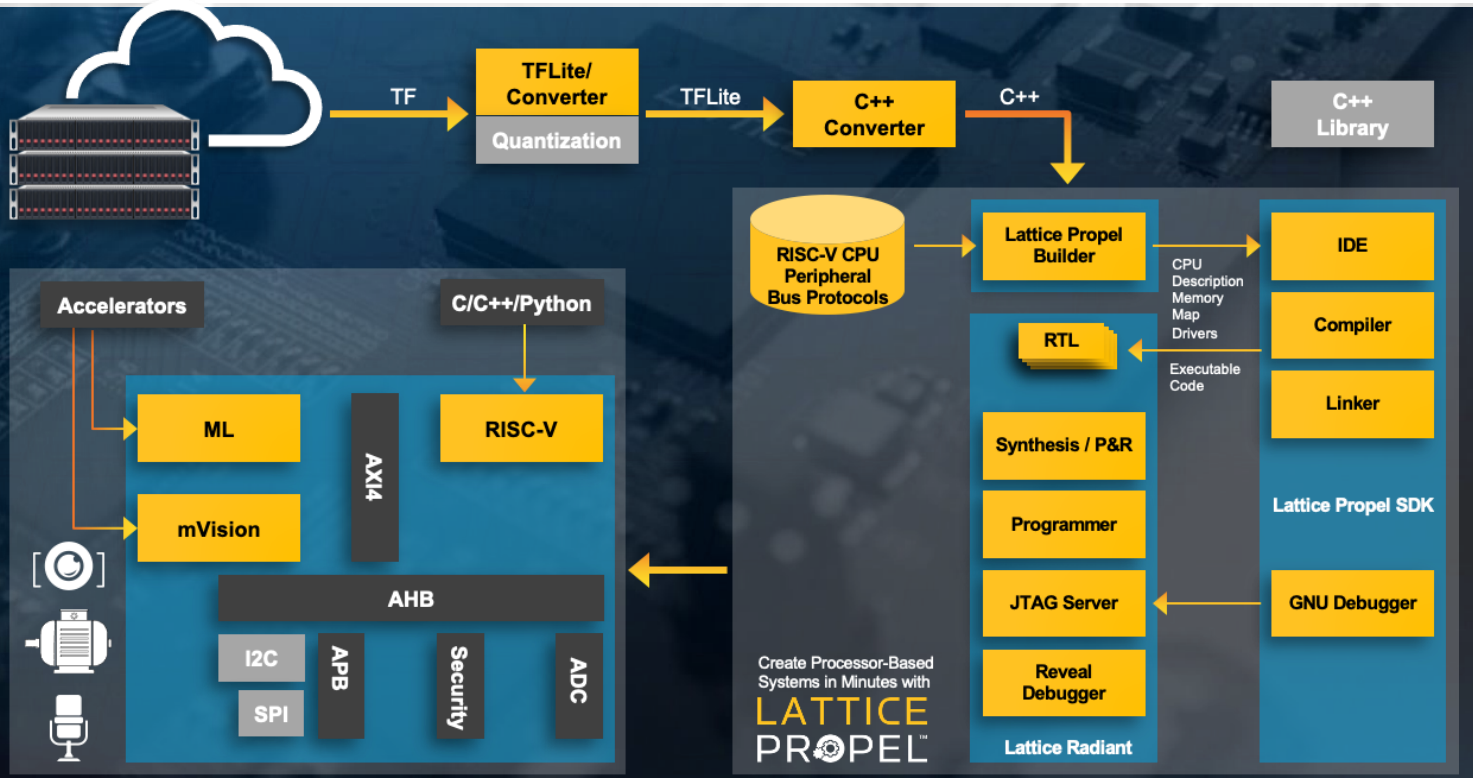
- Configurable 25G SERDES
- Dedicated PCIe® Gen 4 x8 controllers
- Programmable high performance I/O
- High speed memory interfaces up to DDR5



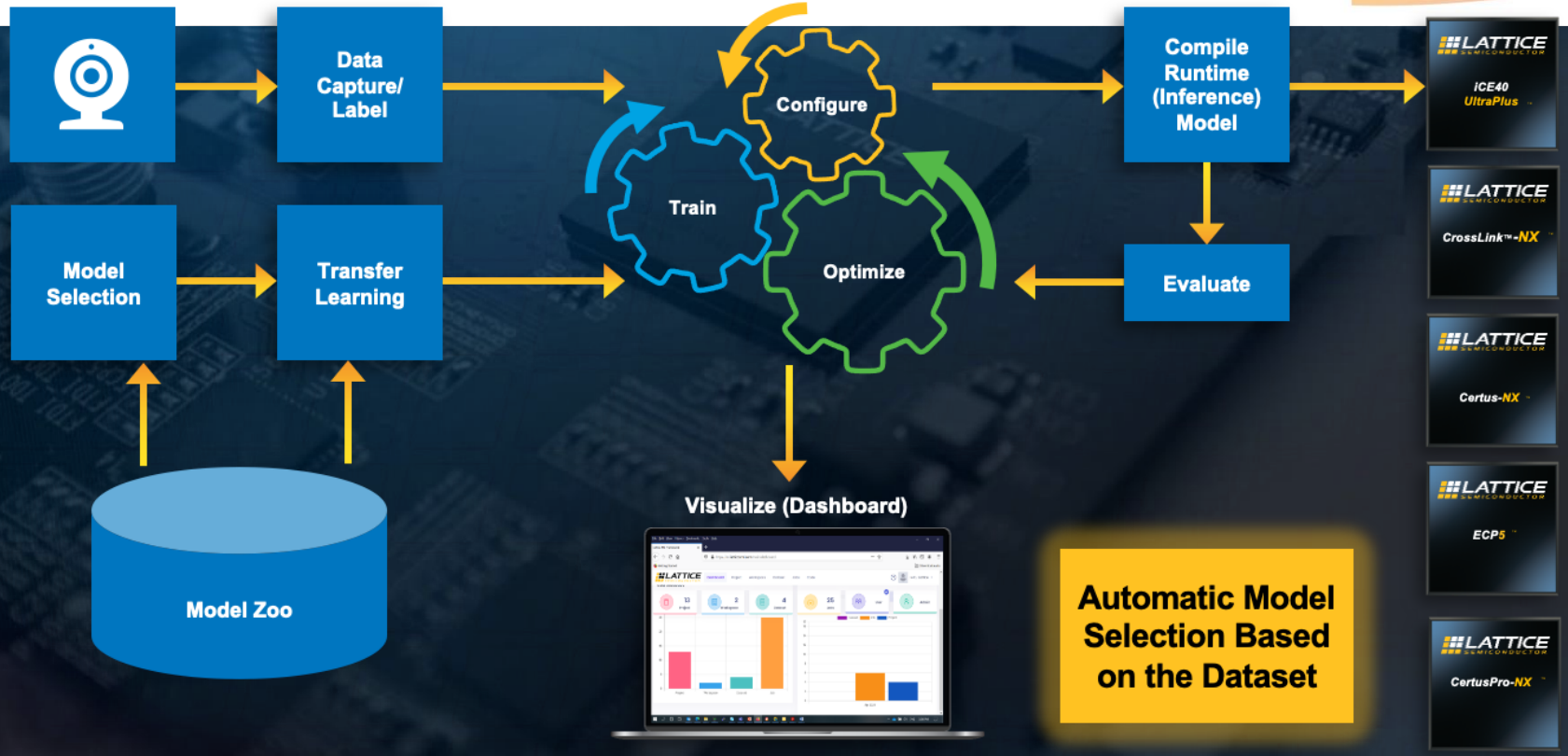
Hardware Optimized Design Methodology



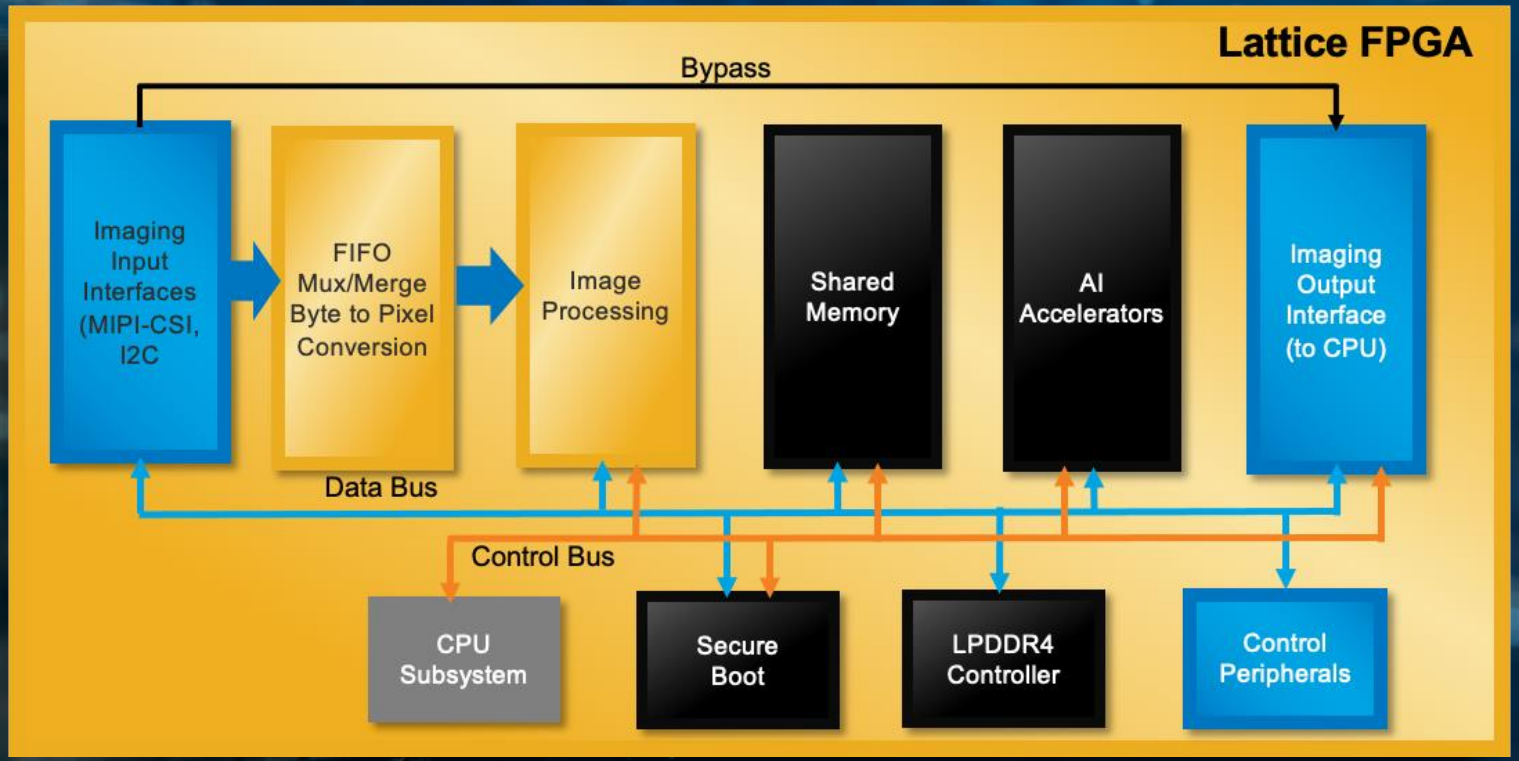
Software Optimized Design Methodology



Lattice sensAI Studio



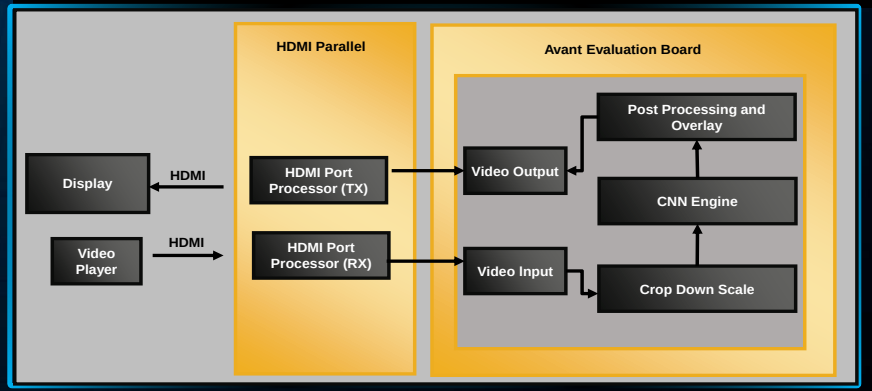
Example FPGA Implementation for Computer Vision



Object Classification – Real Time Video Analysis

Features	
Video input	1080P
Inferencing speed	77 FPS (17x CertusPro-NX)
Power	1.6 W (4x CertusPro-NX)
Processing resolution	480 x 288
NN model	Mobilenet v2

System Block Diagram



FPGA	Engine	# of DSP Engines	# of INT8 Multipliers	FPGA Resources Usage	FPS
Avant 500	Advanced CNN	272	1088	15%	77
CertusPro-NX	Advanced CNN	72	144	32%	10
CrossLink-NX	CNNPlus	18	36	46%	5

Creating Ready for Production Solutions

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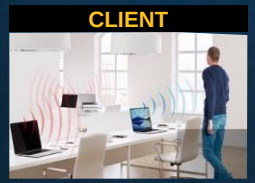
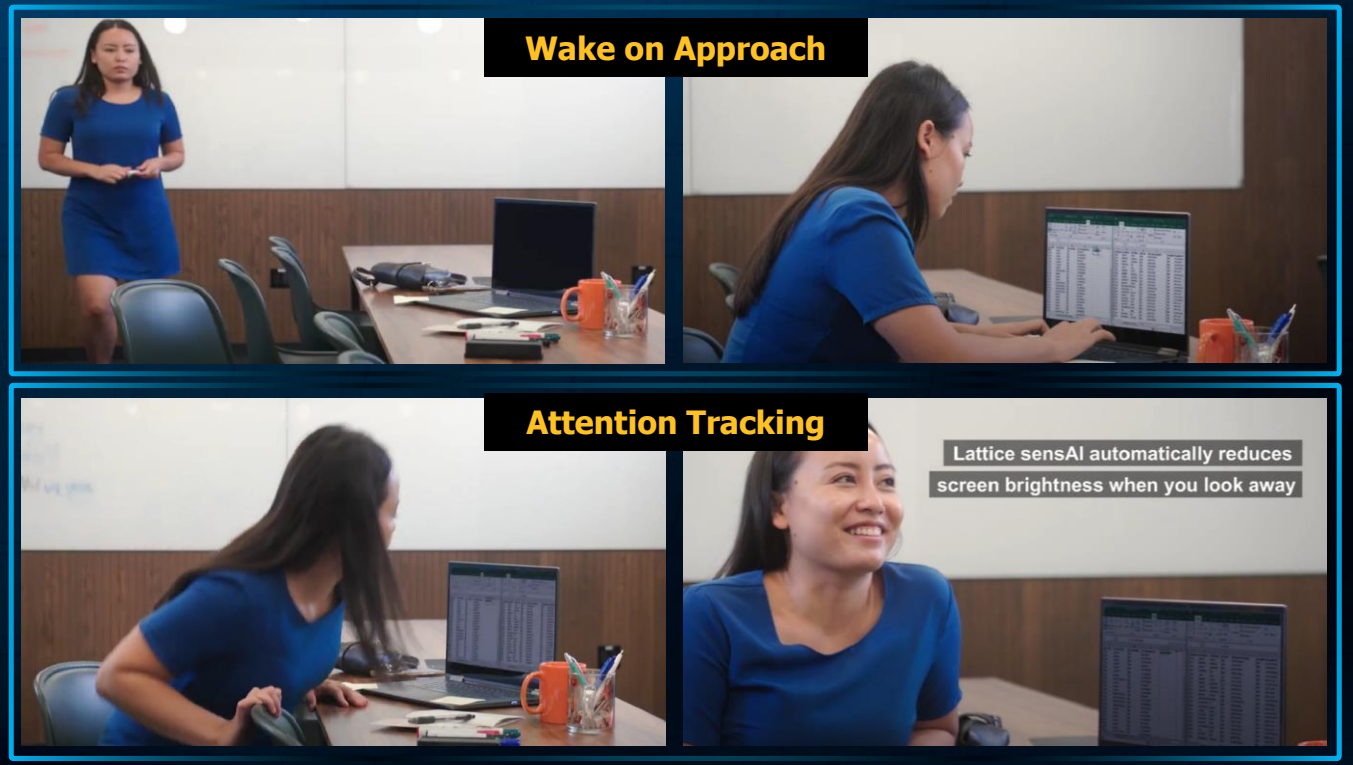


MIRAMETRIX™

- Presence Detection
- Depth Sensing
- 3D Head & Gesture Tracking
- Face ID & Landmarks Tracking
- Eye Feature Detection & Tracking
- Human Skeleton Detection
- Object Detection

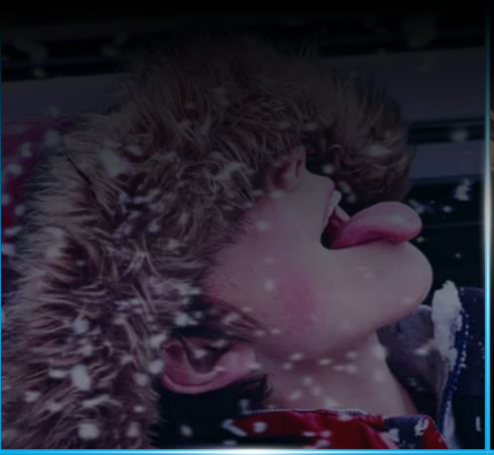
Advanced AI Technology for the Edge

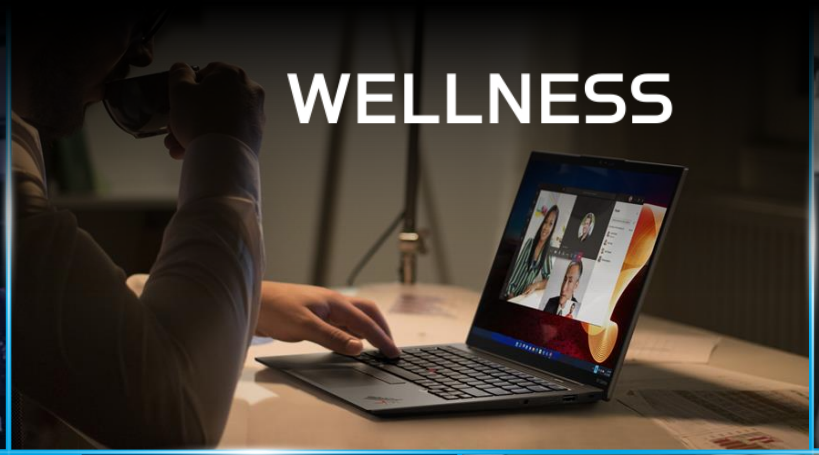
Essential Features

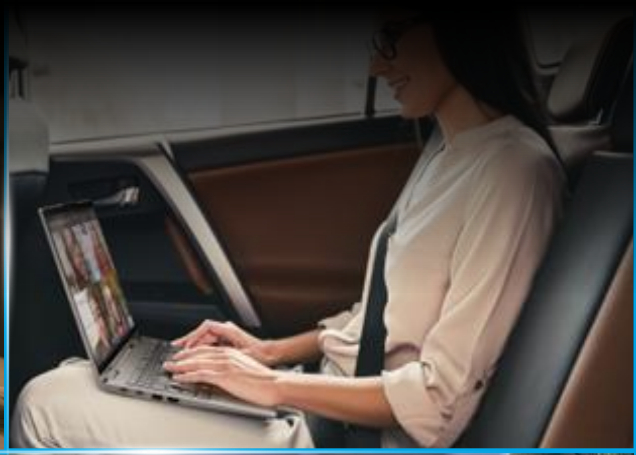


Privacy & Security

WELLNESS







Summary and Takeaways

- Edge AI challenges require adaptable architecture for continued innovation
- FPGAs' programmability allows tinkering with the end-to-end designs before and after production
- A hardware-programable AI accelerator allows systems to evolve with new AI models
- Vision applications need flexible acceleration for the entire pipeline
- New class of mid range FPGAs come with DSP, memory and I/O advancement
- Tools, IPs and examples designs accelerate time to market
- Production-ready solutions can be customized and embedded into different applications

Demos and Additional Resources

The Low Power Programmable Leader